CLAIMS

What is claimed is:

1. A liquid crystal display system comprising:
   a display driver integrated circuit;
   a memory coupled to said display driver integrated circuit; and
   at least one liquid crystal microdisplay coupled to said display driver integrated circuit wherein a frame of video information is written to said memory in a same time period as a previously stored frame of video information is read from said memory more than one time and provided to said at least one liquid crystal microdisplay.

2. The liquid crystal display system as recited in claim 1 wherein said previously stored frame of video information is read from said memory two times to provide a non-inverted and inverted frame of video information to prevent degradation of said at least one liquid crystal microdisplay.

3. The liquid crystal display system as recited in claim 1 wherein said display driver integrated circuit includes:
   an input FIFO;
   a RAM interface unit coupled to said input FIFO and said memory; and
   an output FIFO coupled to said RAM interface unit and said at least one liquid crystal microdisplay.

4. The liquid crystal display system as recited in claim 3 wherein said input FIFO is capable of storing a line of video information corresponding to a largest video format supported by said display driver integrated circuit.

5. The liquid crystal display system as recited in claim 4 wherein said input FIFO is capable of storing 1.5 lines of video information corresponding to said largest video format support by said display driver integrated circuit to ensure that an overflow condition does not occur.

6. The liquid crystal display system as recited in claim 3 wherein said output FIFO is capable of storing a line of video information corresponding to a largest video format supported by said display driver integrated circuit.

7. The liquid crystal display system as recited in claim 6 wherein said output FIFO is capable of storing 1.5 lines of video information corresponding to said largest video format support by said display driver integrated circuit to allow for latency in said RAM interface unit in servicing said output FIFO.

8. The liquid crystal display system as recited in claim 1 wherein said RAM interface unit controls said input FIFO, said memory, and said output FIFO such that said output FIFO has an output frame rate greater than an input frame rate to said input FIFO.

9. The liquid crystal display system as recited in claim 1 wherein said at least one liquid crystal microdisplay comprises:

a first reflective crystal microdisplay coupled to said display driver integrated circuit;

a second reflective crystal microdisplay coupled to said display driver integrated circuit; and

a third reflective crystal microdisplay coupled to said display driver integrated circuit.

10. A method of providing frames of video information to a liquid crystal display comprising the steps of:

providing frames of video information;

identifying a start of an incoming frame of video information;

writing said incoming frame of video information to a memory within a time period having a predetermined duration;

reading a previously stored frame of video information more than one time from said memory during said time period; and

providing said previously stored frame of video information more than one time to the liquid crystal microdisplay.

11. The method as recited in claim 10 further including a step of repeating the following steps for each provided frame of video information:

identifying a start of an incoming frame of video information;

writing said incoming frame of video information to said memory within a time period having said predetermined duration;

reading a previously stored frame of video information more than one time from said memory during said time period; and

providing said previously stored frame of video information more than one time to the liquid crystal microdisplay.

12. The method as recited in claim 10 wherein said steps of writing said incoming frame of video information to a memory within a time period having a predetermined duration and reading a previously stored frame of video information more than one time from said memory during said time period include the steps of:

writing a line of said incoming frame of video information to said memory;

reading more than one line of said previously stored frame of video information from said memory; and

repeating said steps of writing a line and reading more than one line until said incoming frame is written to said memory and said previously stored frame of video information has been read out more than one time.

13. The method as recited in claim 12 wherein said step of writing a line of aid incoming frame of video information to said memory further includes the steps of:

storing said line of said incoming frame of video information in a fifo; and

writing said line stored in said fifo to said memory.

14. The method as recited in claim 12 wherein said step of reading more than one line of said previously stored frame of video information from said memory further includes the steps of:

reading a line from said previously stored frame of video information in said memory;

storing said line in a fifo;

providing said line in said fifo to the liquid crystal microdisplay;

reading at least one more line from said previously stored frame of video information;

storing said at least one more line from said previously stored frame of video information to said fifo; and

providing said at least one more line in said fifo to the liquid crystal micro display.

15. The method as recited in claim 10 further including the steps of:

partitioning said memory into a first area and a second area;

storing said previously stored frame of video information in said first area of said memory; and

storing said incoming frame of video information in said second area of said memory wherein subsequent incoming frames of video information toggle back and forth being written into said first and second areas of said memory.

16. The method as recited in claim 10 further including a step of overwriting said previously stored frame of video information with video information of said incoming frame after said previously stored frame of video information has been read for a final time such that the memory requires less than two frames of storage capability.

17. A frame buffering section of a liquid crystal microdisplay driver integrated circuit for interfacing with a memory comprising:

an input fifo coupled for receiving incoming video information;

an output fifo for providing video information to other circuitry of the liquid crystal microdisplay driver integrated circuit; and

a RAM interface unit coupled to said input fifo, said output fifo, and the memory wherein said RAM interface unit manages writing stored video information in said input fifo corresponding to an incoming frame of video information to the memory and manages reading stored video information from the memory corresponding to a previously stored frame of video information to said output fifo such that a rate at which video information outputs the output fifo is greater than a rate at which video information is input to the input fifo.

18. The frame buffering section of a liquid crystal microdisplay driver integrated circuit for interfacing with a memory as recited in claim 17 wherein the memory is capable of storing two frames of video information.

19. The frame buffering section of a liquid crystal microdisplay driver integrated circuit for interfacing with a memory as recited in claim 17 wherein the input fifo is capable of storing at least one line of video information.

20. The frame buffering section of a liquid crystal microdisplay driver integrated circuit for interfacing with a memory as recited in claim 17 wherein the output fifo is capable of storing at least one line of video information.

21. A method of handling video information for a liquid crystal microdisplay comprising the steps of:

storing video information from an incoming frame into an input fifo;

writing video information stored in said input fifo to a memory;

reading video information from a previously stored frame of video information in said memory to an output fifo;

providing said video information in said output fifo to said liquid crystal microdisplay; and

repeating said steps listed hereinabove such that said incoming frame is written to said memory and said previously stored frame of video information is read out at least once from said memory in a same time period.

22. The method of handling video information for a liquid crystal microdisplay as recited in claim 21 wherein said step of storing video information from an incoming frame into an input fifo further includes a step of storing one line or less of video information into said input fifo.

23. The method of handling video information for a liquid crystal microdisplay as recited in claim 21 wherein said step of storing video information from an incoming frame into an input fifo further includes a step of storing more than one line of video information into said input fifo.